MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(Deemed to be University under Section 3 of UGC Act. 1956)

NAAC A+, NIRF 25 (201-300), NBA Accredited (All eligible B.Tech., MBA & MCA Programs)

EXAMINATION SECTION

ACADEMIC YEAR: 2025-26

Time Table - M.Tech. I Year I Semester - I Mid Term Test - November 2025

TIMINGS: FN: 11:00 A.M to 01:00 PM

AN: 03:00 P.M to 05:00 PM

Date/Day	Session	Computer Science and Engineering (CSE)	VLSI Design and Embedded Systems (VES)
13.11.2025 (Thursday)	**FN**	Advanced Data Structures and Algorithms-25MBCSETC01	CMOS Digital IC Design- 25MBVESTC01
	AN	Modern Database Management Systems-25MBCSETC02	Advanced Microcontrollers and Signal Processors-25MBVESTC02
14.11.2025 (Friday)	**FN**	Research Methodology and IPR-25MBCOMTC01	
	AN	Natural Language Processing- 25MBCSEDC01	FPGA Architectures and Applications-25MBVESDC03
15.11.2025 (Saturday)	**FN**	Big Data Analytics- 25MBCSEDC04	Low Power VLSI Design-25MBVESDC04
	AN	Disaster Management-25MBCIVMC01	Disaster Management- 25MBCIVMC01

Controller of Examinations (I/c)

CONTROLLER OF EXAMINATIONS
Madanapalle Institute of Technology & Science
(Deemed to be University)
MADANAPALLE - 517 325, A. P.

To be read in all the M. Tech-(CSE, VES) I Year I Semester Classrooms

Copy to The File Notice Board HoD-CSE HoD-ECE Transport Incharge

Note: HoD is requested to circulate among the faculty members concerned